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The Conductance- and Capacitance-Frequency Characteristics of the Rectifying Junctions Formed by Sublimation of Organic Pyronine-B on p-Type Silicon

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The rectifying junction characteristics of the organic compound pyronine-B film on a p-type Si substrate has been studied. The pyronine-B has been sublimed on the top of p-Si surface. The barrier height and ideality factor values of 0.79 ± 0.04 and 1.13 ± 0.06 eV for this structure have been obtained from the forward bias current–voltage (*I–V*) characteristics. From the low capacitance-frequency (*C–f*) characteristics as well as conductance–frequency (*G–f*) characteristics, the energy distribution of the interface states and their relaxation time have been determined in the energy range of $(0.53-E_v)$–$(0.79-E_v)$ eV taking into account the forward bias *I–V* data. The interface state density N_{ss} ranges from $4.93 \times 10^{10}\,cm^{-2}\,eV^{-1}$ in $(0.79-E_v)$ eV to $3.67 \times 10^{13}\,cm^{-2}\,eV^{-1}$ in $(0.53-E_v)$ eV. Furthermore, the relaxation ranges from 3.80×10^{-3} s in $(0.53-E_v)$ eV to 4.21×10^{-4} s in $(0.79-E_v)$ eV. It has been seen that the interface state density has an exponential rise with bias from the midgap towards the top of the valence band. The relaxation time shows a slow exponential rise with bias from the top of the valence band towards the midgap. © 2002 Elsevier Science (USA)

Key Words: **organic–inorganic semiconductor contacts; heterojunctions; semiconductor-semiconductor contacts; Schottky contacts; Schottky barrier heights.**

1. INTRODUCTION

The Schottky contacts have an important role in modern electronics (1–5). In addition, the interface states and interfacial oxide layer between the inorganic semiconductor and deposited material used for the rectifying contact formation play an important role in the determination of the Schottky barrier height (SBH) and other characteristics parameters of the devices (6–14). The electrical and photoelectrical properties of polymeric (5–10) and non-polymeric organic compounds (11–14) have been the investigation subject for more than 2–3 decades. Due to the stability of non-polymeric organic compounds (organic low molecular weight compounds), they have been employed particularly in the electronics devices (11–15). Forrest *et al.* (11) reported the current–voltage (*I–V*) characteristics of the non-polymeric organic thin films (3,4,9,10-perylenetetracarboxylic dianhydride–PTCDA) sublimed on p-type Si substrate. Again, Sharma *et al.* (13) have studied the *I–V* characteristics in dark as well as under illumination and capacitance–voltage (*C–V*) characteristics in dark of the sandwich devices having ITO/pyronine-G(Y)/Al and ITO/pyronine-G(Y)/In prepared by the spin coating technique. Recently, Böhler *et al.* (14) have investigated microwave applications of organic-on-inorganic heterostructure diodes based on crystalline thin PTCDA films on InP semiconductor.

In the present study, the pyronine-B/p-Si/Sn structures are directly formed by vacuum sublimation of the non-polymeric organic compound pyronine-B (organic low molecular weight compound) onto the top of p-Si surface. The characteristic parameters of the fabricated pyronine-B/p-type Si/Sn diodes were calculated using the forward-bias *I–V*, capacitance–frequency (*C–f*) and conductance–frequency (*G–f*) measurements. The forward-bias *C–f*) and *G–f* measurements give the important information about the interface state energy distribution of Schottky barrier diodes (SBDs). In general, the *C–f* and *G–f* plots in the idealized case are frequency independent (15–30). However, this idealized case is often disturbed due to the presence of the interface states at the interfacial layer and semiconductor interface (15–30).

2. EXPERIMENTAL PROCEDURE

The samples were prepared using mirror cleaned and polished (as received from the manufacturer) p-type Si

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wafers with (100) orientation and 5–10 Ω cm resistivity. The wafer was chemically cleaned using the RCA cleaning procedure (i.e., a 10 min boil in $NH_3 + H_2O_2 + 6H_2O$ followed by a 10 min boil in $HCl + H_2O_2 + 6H_2O$). The native oxide on the front surface of the substrate was removed in $HF{:}H_2O$ (1:10) solution and finally, the wafer was rinsed in de-ionized water for 30 s. Before forming organic layer on the p-type Si substrate, the ohmic contact was made by evaporating Al on the back of the substrate, followed by a temperature treatment at 570°C for 3 min in N_2 atmosphere. Then, the polycrystalline pyronine-B was purified by gradient sublimation in a quartz tube heated between 350°C and 100°C at opposite ends in a vacuum of 10^{-2} Torr. The p-type Si substrate was inserted into a vacuum system of 10^{-5} Torr, and the pyronine-B was sublimed heating the pyronine-B source to ~450°C using a resistance heater. The deposition rate was between 60 and 90 Å/s, as determined using a quartz-crystal thickness monitor. The distance from the evaporation source to the p-type Si substrate was maintained at 12 cm and the substrate temperature was about 30°C. The thickness of pyronine-B film on the substrate was between 650 and 1000 Å across the full wafer surface and uniform. Finally, top metal contact, Sn, was deposited through a shadow mask. Thus, an Sn/pyronine-B/p-Si diode was obtained. The area of circular Schottky contact was $1.43 \times 10^{-6}\,m^2$. All metallic surfaces were cleaned by acetone and methanol before the processes. The *I–V* and *C–V–f* and *G–V–f* measurements of the devices were performed using a Keithley 487 Picoammeter/Voltage Source and a HP 4192A *LF* Impedance Analyzer, respectively, at room temperature and in dark.

3. RESULTS AND DISCUSSION

3.1. The Current–Voltage Characteristics

We presented the fabrication of the non-polymeric organic compound pyronine-B/p-type Si/Sn diodes. The molecule structure of the pyronine-B is given in Fig. 1. In a

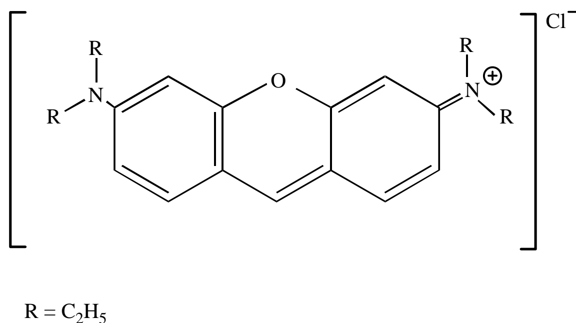

FIG. 1. Molecular structure of pyronine-B.

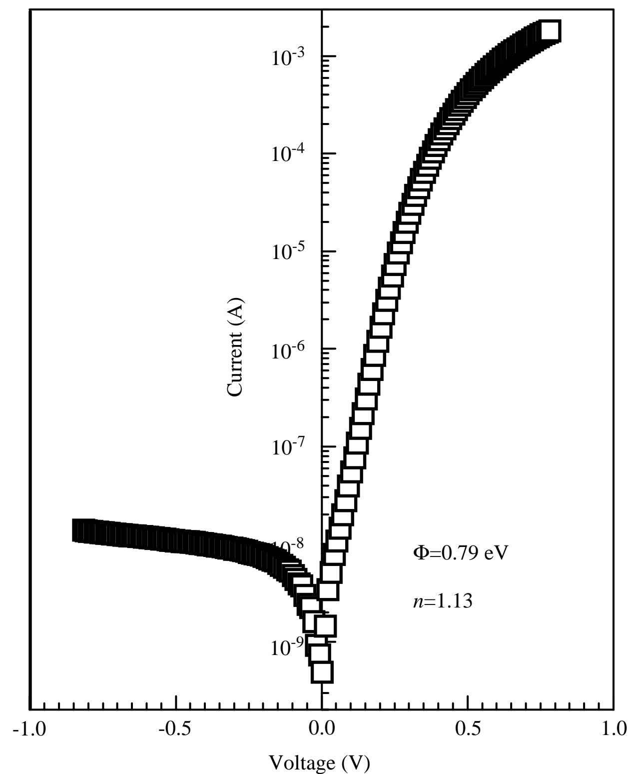

FIG. 2. Forward and reverse bias current versus voltage characteristics at room temperature of the rectifying Sn/pyronine-B/p-type Silicon junction formed by sublimation.

previous study by us (29), the pyronine-B/p-Si structure is directly formed adding 7.0 μL of the pyronine-B solution of 1×10^{-6} M in methanol on a p-type silicon substrate, and then evaporating the solvent. As is mentioned above, in the present study, the pyronine-B has been sublimed onto the top of p-Si surface.

As can be seen from Fig. 2, the current–voltage characteristics of the Sn/pyronine-B/p-Si Schottky contact show the rectifying behavior and the reverse curve exhibits the excellent saturation. Therefore, we have used the simple thermionic emission theory to obtain the characteristic parameters of the device (28–33). We have made the error calculation by considering parameters of the other dots of the junction and determined the junction parameters within an error of 5%. Thus, we have calculated the values of about 0.79 ± 0.04 eV and 1.13 ± 0.06 for the zero bias effective barrier height $\Phi_{b,o}$ and ideality factor n of the Sn/pyronine-B/p-Si Schottky contact from the *y*-axis intercept and slope of the linear region of the semilog-plot of the experimental forward bias *I–V* data (the effective Richardson constant equals to $32\,A/cm^2\,K^2$ for p-type Si (30,31)). It should be known that $\Phi_{b,o}$ is the contact potential barrier that exists at the interface between the organic and inorganic layers, that is, at the pyronine-B/p-Si interface.

The value of 1.13 of n indicates the presence of a thin interfacial insulator layer (an native oxide layer) at the pyronine and Si interface (28–33). The interface oxide layers can inevitably be formed by water or vapor adsorbed onto the surface of the p-type Si substrate before sublimation of the pyronine-B (28–33). Therefore, the pyronine-B/p-Si contacts formed under these conditions are not intimate contact because an interfacial layer of atomic dimensions inevitably separates the pyronine and Si (28–33). For a sufficiently thick interface layer, the interface states are in equilibrium with the inorganic semiconductor (p-Si substrate) and they cannot interact with the pyronine-B (the organic semiconductor) (15, 28–33). As can be seen from Fig. 2, the curvature downward in the forward I–V plots at sufficiently large applied voltage is due to the substrate series resistance and interface state continuum (28–33). That is, it can be concluded that the barrier height determined from the I–V characteristics is controlled by the interface states in equilibrium with the inorganic semiconductor.

We reported the barrier height and ideality factor values of 0.65 eV and 1.51 for the Sn/pyronine-B/p-Si structure in the previous work (29), in which the Sn/pyronine-B/p-Si structure had been fabricated by placing the pyronine-B solution of 1×10^{-6} M in methanol on a substrate of the same p-type silicon. As can be seen, the barrier height value of the Sn/pyronine-B/p-Si structure formed by the sublimation is larger than that of the structure formed by the solution, and ideality factor value smaller. As is mentioned above, it can be concluded that the barrier height and ideality factor determined from the I–V characteristics is controlled by the interface states in equilibrium with the inorganic semiconductor. As will be explained below, the interface state density N_{ss} from the capacitance and conductance (C–G) measurements as a function of the frequency (f) for the structure by the sublimation ranges from 4.93×10^{10} to $3.67 \times 10^{13}\,cm^{-2}\,eV^{-1}$, from the midgap towards the top of the valance band. The density of N_{ss} from the C–G–f measurements for the structure by the solution ranges from 9.44×10^{11} to $5.07 \times 10^{13}\,cm^{-2}\,eV^{-1}$, from the midgap to the top of the valence band (the calculation by means of the C–G–f method for the structure by the solution is not given in the previous work (29), the calculation by Schottky capacitance spectroscopy method using only C–f measurements is given there). As can be seen, the interface state density from the midgap towards the top of the valence band is more dominant for the structure obtained by the solution. In practice, when a forward bias is applied to a Schottky diode which is under the effects of the interfacial layer parameters, the quasi-Fermi level (imref) for the majority carriers rises on the semiconductor side. Thus, most of the electrons will be injected directly into the organic material by forming a thermionic emission current, while some of them are trapped by the interface states. The charge-capture process results in an increase or the shift of the effective barrier height with the bias voltage, thereby reducing the diode current, and thus the I–V characteristics become non-ideal. Therefore, the I–V curve (Fig. 2) of the structure by the sublimation is more linear and ideal than that of the structure by the solution (Fig. 2 in Ref. (29)). Moreover, the sublimed pyronine-B may adhere well to the p-type silicon substrate, that is, the sublimation may improve adhesion with respect to the pyronine-B solution.

3.2. The Conductance- and Capacitance-Frequency Characteristics

Figures 3 and 4 show the measured capacitance and conductance as a function of the frequency with steps of 0.02 V as a parameter. As has been seen from Fig. 3, the measured capacitance remained almost constant up to a certain value of the frequency in the lower side of the frequency scale. The higher values of capacitance at low frequencies are due to excess capacitance resulting from the interface states in equilibrium with the p-Si that can follow the ac signal. As the frequency was increased further, the diode capacitance first decreased and then became almost constant. A near constant value of the capacitance resulting in the intermediate frequency region means the case where a much small part of the interface states can only follow the signal.

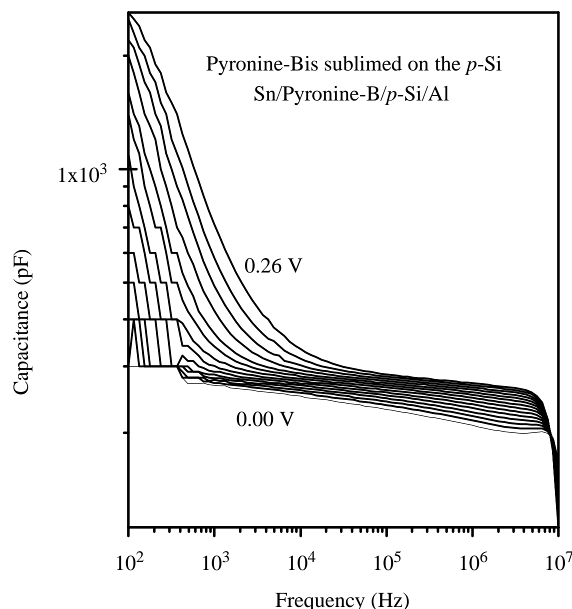

FIG. 3. Experimental forward-bias capacitance plot as a function of the frequency with bias voltage as a parameter at room temperature of the rectifying Sn/pyronine-B/p-type Silicon junction formed by sublimation (0.00–0.26 V with steps of 0.02 V).

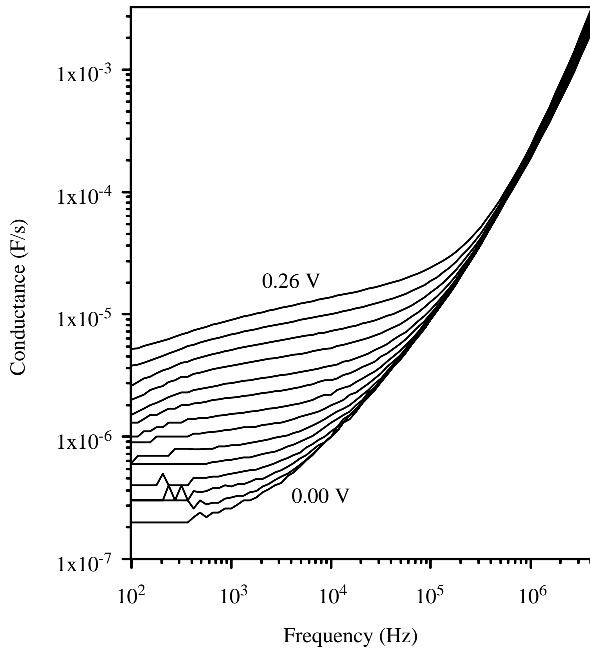

FIG. 4. Experimental forward-bias conductance plot as a function of the frequency with bias voltage as a parameter of the Sn/pyronine-B/p-Si Schottky barrier diode (0.00–0.26 V with steps of 0.02 V) at room temperature.

The low-frequency–capacitance and –conductance characteristics can be used to characterize the interface states at Schottky barrier structures (15–30). The equivalent circuit describes the capacitance C_{ss} and conductance G_{ss} of the interface states that are in parallel to the capacitance of the depletion region C_{sc} and in series with interfacial layer capacitance C_i. Now, let us calculate the density distribution of the interface states from the experimental capacitance–frequency and conductance–frequency measurements of the Sn/pyronine-B/p-Si diode.

According to Nicollian and Goetzberg (16), the interface state conductance for a MIS structure can be described as

$$G_{ss} = \frac{AqN_{ss}}{2\tau} \ln(1 + w^2\tau^2), \qquad [1]$$

where τ is the time constant of the interface states which can be written as

$$\tau = \frac{1}{v_{th}\sigma N_A} \exp\left(\frac{qV_d}{kT}\right), \qquad [2]$$

with N_{ss} being the interface state density, σ the cross section of interface states, v_{th} the thermal velocity of carrier and N_A the doping concentration and A the contact area.

The conductance of the interface states G_{ss} is given by (17)

$$G_{ss} = \frac{qJ_{dc}}{kT} \frac{C_i(C - C_{HF})}{(C - C_{HF})^2 + (G/w)^2} \qquad [3]$$

with

$$\frac{1}{C_{HF}} = \frac{1}{C_i} + \frac{1}{C_{sc}}, \qquad [4]$$

where G and C are the measured diode conductance and capacitance, respectively, C_i is the capacitance of the interfacial layer formed from the native oxide and pyronine-B between Sn and p-Si, and determined from the high-frequency (HF) values of C. As can be seen from Eq. [4], C_i is in series with the space charge capacitance C_{sc} of the inorganic semiconductor (12). J_{dc} is the experimentally measured forward-bias current density. Figure 5 shows the high-frequency (HF) capacitance–voltage plot of the Sn/Pyronine-B/p-Si structure at room temperature. The accumulation region of the HF C–V characteristic measured at 500 kHz for the structure has given a value of about $C_{ox} = 1050$ pF.

Furthermore, in a p-type semiconductor, the energy of the interface states E_{ss} with respect to the top of the valence band at the surface of the semiconductor is given by (32)

$$E_{ss} - E_v = q\Phi_b - qV. \qquad [5]$$

The quantity G_{ss}/w given in Fig. 5 was calculated from the experimental forward bias J_{dc} (Fig. 2), C (Fig. 3) and G (Fig. 4) values for the voltages of Figs. 3 and 4 with the help of Eq. [3]. The G_{ss}/w versus $\ln(w)$ behavior can be explained by the presence of an almost continuous distribution of interface state energy levels (Fig. 6). At a given bias, the Fermi level fixes the occupancy of these interface traps levels, and a particular interface charge density will be at the Si surface which determines the time constant of the related interface states. When the ac signal

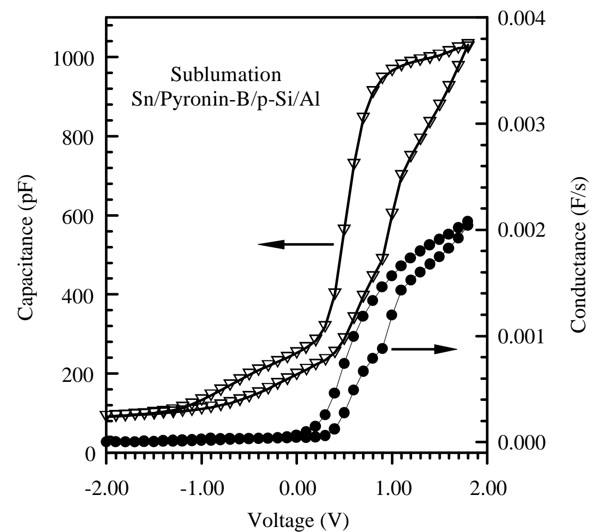

FIG. 5. High-frequency capacitance–conductance–voltage plots of the Sn/Pyronine-B/p-Si/Al structure at room temperature.

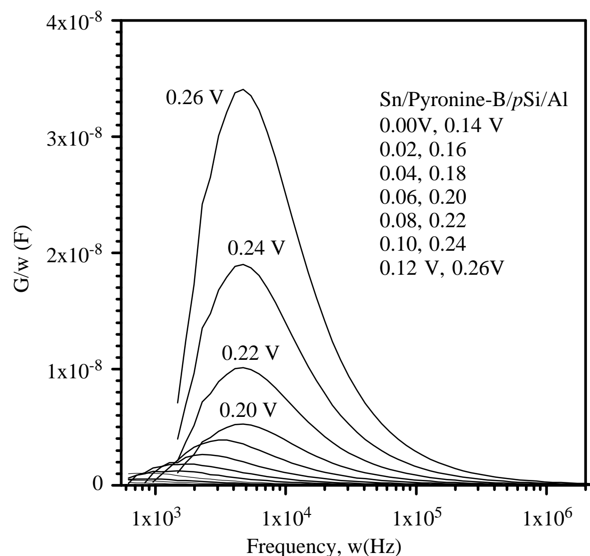

FIG. 6. G_{ss}/w versus w characteristics obtained from the experimental data in Figs. 3 and 4.

TABLE 1
The Experimental Interface-State Density N_{ss} and Relaxation Time τ Obtained from Conductance- and Capacitance-Frequency Characteristics of the Rectifying Sn/Pyronine-B/p-Type Silicon Junctions Formed by Sublimation of Pyronine-B

V (V)	$E_c - E_{ss}$ (eV)	$N_{ss} \times 10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$	$\tau \times 10^{-3}$ (s)
0.00	0.79	0.493	3.80
0.02	0.77	0.734	3.65
0.04	0.75	2.370	3.51
0.06	0.73	4.68	3.72
0.08	0.71	5.85	2.34
0.10	0.69	11.2	2.34
0.12	0.67	13.2	1.38
0.14	0.65	19.5	1.15
0.16	0.63	28.3	0.83
0.18	0.61	41.8	0.60
0.20	0.59	57.5	0.43
0.22	0.57	109	0.42
0.24	0.55	204	0.42
0.26	0.53	367	0.42

corresponds to this time constant, the peak loss associated to the interface trap levels will occur. If the frequency is slightly different from the time constant, losses are reduced because trap levels either do not respond or the response occurs at a different frequency. Therefore, the loss peak is a function of frequency. Moreover, the peak value depends on the capture rate, that is, on the interface state level occupancy that is determined by the applied bias (16–22).

The curves go through maxima at $w\tau = 1{,}98$ with values of $(G_{ss}/w)_{max} = 0{,}40qAN_{ss}$. The ordinates and frequencies of the maxima yield therefore density of the interface states

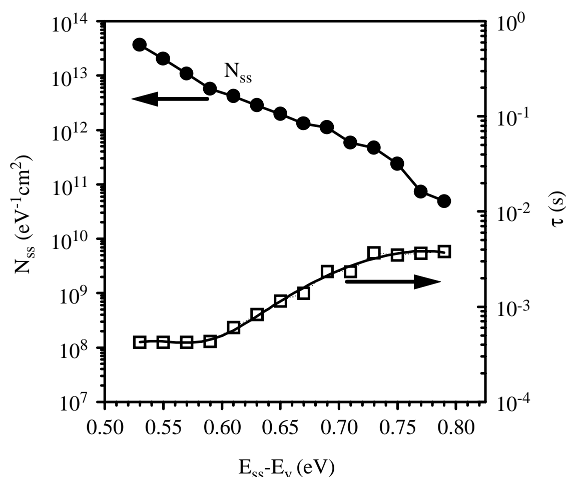

FIG. 7. Density distribution curves of the interface states and their time constants in the energy range $(0.53\text{-}E_v)-(0.79\text{-}E_v)$ eV obtained from the experimental G_{ss}/w versus w characteristics for the Sn/pyronine-B/p-Si Schottky diode taking into account the forward-bias I–V data at room temperature.

and their time constant τ. Then, the dependence of N_{ss} and τ on the bias was converted to a function of E_{ss} using Eq. [5] and is shown in Fig. 7 and Table 1. As can be seen from Fig. 7, the interface-state density N_{ss} ranges from $4.93 \times 10^{10}\,\mathrm{cm^{-2}\,eV^{-1}}$ in $(0.79\text{-}E_v)$ eV to $3.67 \times 10^{13}\,\mathrm{cm^{-2}\,eV^{-1}}$ in $(0.53\text{-}E_v)$ eV. Furthermore, the relaxation ranges from 3.80×10^{-3} s in $(0.53\text{-}E_v)$ eV to 4.21×10^{-4} s in $(0.79\text{-}E_v)$ eV. It has been seen that the interface state density has an exponential rise with bias from the midgap towards the top of the valence band. The relaxation time shows a slow exponential rise with bias from the top of the valence band towards the midgap, as reported by some authors for metal/Schottky diodes (17–19). Thus, it can be said the relaxation time to be bias-dependent.

In conclusion, the pyronine-B has been sublimed onto the top of p-Si substrate and formed the Sn/pyronine-B/p-Si structures. $\Phi_{b,o}$ and n values of 0.79 ± 0.04 eV and 1.13 ± 0.06 for the device have been obtained from the forward-bias I–V data. The energy distribution of the interface states and their relaxation time have been determined from the C–f characteristics as well as G–f characteristics taking into account the forward-bias I–V data, between the midgap and valence band top. The energy distribution of the interface states and relaxation time show an exponential rise with bias.

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